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NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER
SHAN, APRIL YING

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2135	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 10/714,565	**Applicant(s)** WATT ET AL.
	Examiner April Y. Shan	**Art Unit** 2135

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2007*.

2a)☒ This action is **FINAL**. 2b)□ This action is non-final.

3)□ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11 and 13-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)□ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11 and 13-21* is/are rejected.

7)□ Claim(s) _____ is/are objected to.

8)□ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)□ The drawing(s) filed on _____ is/are: a)□ accepted or b)□ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)□ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)□ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)□ All b)□ Some * c)□ None of:

1.□ Certified copies of the priority documents have been received.

2.□ Certified copies of the priority documents have been received in Application No. _____.

3.□ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) □ Notice of References Cited (PTO-892)

2) □ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date *4/26/2007*.

4) □ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) □ Notice of Informal Patent Application

6) □ Other: _____.

DETAILED ACTION

Response to Amendment

1. The Applicant's amendment, filed 26 April 2007, has been received, entered into the record, respectfully and fully considered.

2. As a result of the amendment, claims 1, 3-11, 13-14, 18 and 20-21 have been amended. Claims 2 and 12 are canceled. Claims 1, 3-11 and 13-21 are now presented for examination.

3. Any objection/rejections not repeated below for record are withdrawn due to Applicant's amendment.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1, 3-11 and 13-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As per **claims 1 and 11**, the Applicant recites "...stored in a **programmable** exception trap mask register....". The examiner carefully and respectfully reviewed the original disclosure, the Applicant discloses on page 27, lines 11-12 of the original disclosure, "Figure 16 also illustrates that the **flags** for the different exception types within the exception trap mask register are **programmable**...". The original disclosure only discloses the flags within the exception trap mask register are programmable, **not** the register itself is programmable. Therefore, the examiner finds no support in the original disclosure "...stored in a **programmable** exception trap mask register" as recited in claims 1 and 11.

As per **claim 21**, "...embodied in a tangible medium and executable on a data processing apparatus" is not clearly defined/supported in the original disclosure. Applicant is required to point out where this new claim limitation is in the original disclosure and please note no new matter should be added in the original disclosure in addressing the claim rejection.

Any claim not specifically addressed, above, is being rejected as incorporating the deficiencies of a claim upon which it depends.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 11 and 13-21 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 11 and 13-20 are directed to a method of processing data. The examiner respectfully asserts that the claimed subject matter does not fall within the statutory classes listed in 35 USC 101. The claimed steps do not result in a tangible result. Claims 11 and 13-20 are rejected as being directed to an abstract idea (i.e., producing non-tangible result) [tangible requirement does require that the claim must recite more than a 101 judicial exception, in that the process must set forth a practical application of that 101 judicial exception to produce a real-world result, Benson, 409 U.S. at 71-72, 175 USPQ at 676-77).

With respect to **claim 21**, the Applicant's efforts to overcome the rejection is acknowledged. Now, the computer program product embodied in a tangible medium. However, the rest of newly added claim limitation "and executable on a data processing apparatus to..." is still non-statutory. It appears to the examiner that the newly added claim limitation is optional, which means the method is not always executed. Additionally, the claimed computer program **still** does not result in a tangible result. Claim 21 is rejected as being directed to an abstract idea (i.e., producing non-tangible result) [tangible requirement does require that the claim must recite more than a 101 judicial exception, in that the process must set forth a practical application of that 101 judicial exception to produce a real-world result, Benson, 409 U.S. at 71-72, 175 USPQ at 676-77).

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 4-11 and 14-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Christie et al. (U.S. Patent No. 7,165,135).

As per **claims 1 and 11**, Christie et al. discloses an apparatus/method for processing data, comprising:

a processor ("a secure execution mode-capable processor" – e.g. col. 4, lines 30-31) operable in a plurality of modes ("the SEM-capable processor operating in a secure user mode and a secure kernel mode in addition to the normal user mode and normal kernel mode" – e.g. col. 4, lines 13-15 and "...two modes within a normal execution mode or protection domain: Normal Kernel Mode and Normal User Mode.." – e.g. col. 4, lines 32-37) and a plurality of domains ("Normal User Domain 1010, Normal Kernel Domain 1020, Secure User Domain 1030 and Secure Kernel Domain 1040" – e.g. fig. 1) said plurality of domains comprising a secure domain and a non-secure domain ("...secure execution mode refers to any mode of processor execution during which SEM is enabled...non-secure execution mode refers to any mode of processor execution during which SEM is disabled" – e.g. col. 4, lines 45-51) said plurality of modes including:

at least one secure mode being a mode in said secure domain ("...SK domain 1040, SEM may allow Security Kernel 1021 full access to all platform resources and in addition may give exclusive control of those resources to Security Kernel 1021. The SK domain 1010 may be characterized by a processor running in Kernel mode (i.e. CPL =0) and also in TX mode, which may also be referred to as a secure kernel mode" – e.g. col. 5, lines 23-29); and

at least one non-secure mode being a mode in said non-secure domain ("NU 1010 domain may be characterized by a processor running in normal user mode (i.e. CPL =3) and not in trusted execution (TX) mode...." – e.g. col. 4, lines 52-64);

wherein

when said processor is executing a program in a secure mode said program has access to secure data which is not accessible when said processor is operating in a non-secure mode ("In the SK domain 1040, SEM may allow Security Kernel 1021 full access to all platform resources and in addition may give exclusive control of those resources to Security Kernel 1021..." – e.g. col. 5, lines 23-29 and "The NU 1010 domain may be characterized by a processor running in normal user mode (i.e. CPL =3) and not in trusted execution (TX) mode...Under SEM, such applications are however prevented from accessing the memory of applications residing in the SU domain 1030, or the memory containing Security Kernel 1021 in the SK domain 1040...." – e.g. col. 4, lines 52-64);

said processor is responsive to one or more exception conditions for triggering exception processing (e.g. col. 9, lines 24 - 43); and said processor being responsive to one or more parameters stored in a programmable exception trap mask register, said one or more parameters ("...Redirection of interrupts in exception logic 170 may be enabled and disabled depending on the state of a SEM enable signal 401...In one embodiment, SEM enable signal 401 may be derived from **an SEM enable flag** (not shown) in **a designated control register or a model specific register** that may be asserted during a secure initialization process" – e.g. col. 10, line 12 – col. 11, line 8 and col. 11, line 57- col. 12, line 4) specifying which of said exceptions should be handled by a secure mode exception handler executing in a secure mode and which of said exceptions should be handled by an exception handler executing in a mode within a current one of said secure domain and said non-secure domain when that exception occurs (e.g. abstract, col. 9, lines 44-61, col. 10, line 31 – col. 11, line 20, col. 11, lines 40-47 and col. 11, line 57 – col. 12, line 4).

As per **claims 4 and 14**, Christie et al. discloses an apparatus/method as applied above in claims 2 and 12. Christie et al. further discloses comprising a configuration controlling coprocessor associated with said processor (e.g. col. 6, line 55 – col. 7, line 61) and wherein said exception trap mask register is a register within said configuration controlling coprocessor (e.g. col. 6, line 55 – col. 7, line 61).

As per **claims 5 and 15**, Christie et al. discloses an apparatus/method as applied above in claims 1 and 11. Christie et al. further discloses wherein at least one of said parameters is a signal value provided at a hardware input to said processor (e.g. col. 10, lines 14-19).

As per **claims 6 and 16**, Christie et al. discloses an apparatus/method as applied above in claims 1 and 11. Christie et al. further discloses wherein said secure exception handler is part of a secure operating system operable in said secure mode (e.g. col. 8, lines 33-56 and col. 9, lines 24-43).

As per **claims 7 and 17**, Christie et al. discloses an apparatus/method as applied above in claims 1 and 11. Christie et al. further discloses wherein said non-secure exception handler is part of a non-secure operating system operable in said non-secure mode (e.g. e.g. col. 8, lines 33-56 and col. 10, lines 47-57).

As per **claims 8 and 18**, Christie et al. discloses an apparatus/method as applied above in claims 1 and 11. Christie et al. further discloses wherein said processor is also operable in a monitor mode and any switching between a secure mode and a non-secure mode required for handling of an exception as specified by said parameters takes place via said monitor mode, said processor being operable at least partially in said monitor mode to execute a monitor program to manage switching between said secure mode and said non-secure mode (e.g. col. 5, lines 30-51).

As per **claims 9 and 19**, Christie et al. discloses an apparatus/method as applied above in claims 8 and 18. Christie et al. further discloses wherein said monitor program may change said parameters to determine where an exception should be handled (e.g. col. 10, lines 31- 46).

As per **claims 10 and 20**, Christie et al. discloses an apparatus/method as applied above in claims 8 and 18. Christie et al. further discloses wherein said processor includes a register bank (e.g. col. 7, lines 59-61) and said monitor program is operable to flush at least a portion of said register bank shared between said secure mode and said non-secure mode when switching from said secure mode to said non-secure mode such that no secure data held within said register bank may pass from said secure mode to said non-secure mode other than as permitted by said monitor program (e.g. col. 7, lines 31-61, col. 9, lines 14-16 and col. 11, lines 35-37).

As per **claim 21**, Christie et al. discloses the claimed method as applied above in claim 11. Therefore, Christie et al. discloses the claimed computer program product having a computer program for carrying out the method to control a data processing apparatus.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

12. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claims 3 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Christie et al (U.S. Patent No. 7,165,135).

As per **claims 3 and 13**, Christie et al. discloses an apparatus/method as applied above in claims 2 and 12.

Christie et al. further disclosed in col. 7, lines 31-43, “System memory 110 is configured to store program instructions and data that is frequently used by SEM processor 100....In addition, system memory 110 may be partitioned into a trusted portion and an untrusted portion. The security kernel resides in the trusted portion of system memory 110." To a person with ordinary skill in the art at the time of the invention, an exception trap mask register is memory to hold data item.

At the time of the invention it would have been obvious to a person of ordinary skill in the art that said exception trap mask register is writable when said processor is in a secure mode (trusted portion and have security kernel resides on disclosed by Christie et al.) and said exception trap mask register is non-writable when said processor is in a non-secure mode (untrusted portion disclosed by Christie et al.).

The motivation of doing so would have been "...desirable to improve security and thereby possibly make x86 architecture system less vulnerable to such access", as taught by Christie et al. (col. 2, lines 47-67)

Double Patenting

15. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422

F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

16. Claims 1, 5-8, 11, 15-18 and 21 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-11 of U.S. Patent No. 7,117,284. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1, 5-8, 11, 15-18 and 21 encompass the same subject matter as claims 1-11 the U.S. Patent No. 7,117,284.

Claim 1 recites Apparatus for processing data, said apparatus comprising: a processor operable in a plurality of modes and a plurality of domains, said plurality of domains comprising a secure domain and a non-secure domain, said plurality of modes including: at least one secure mode being a mode in said secure domain; and at least one non-secure mode being a mode in said non-secure domain; wherein when said processor is executing a program in a secure mode said program has access to secure data which is not accessible when said processor is operating in a non-secure mode; said processor is responsive to one or more exception conditions for triggering exception processing; and said processor being responsive to one or more parameters specifying which of said exceptions should be handled by a secure mode exception handler executing in a secure mode and which of said exceptions should be handled by an exception handler executing in a mode within a current one of said secure domain and said non-secure domain when that exception occurs (claim 1 of the U.S. patent 7,117,284)

Claim 5 recites Apparatus as claimed in claim 1, wherein at least one of said parameters is a signal value provided at a hardware input to said processor (claim 5 of the U.S. Patent 7,117,284)

Claims 6-7 recite Apparatus as claimed in claim 1, wherein said secure exception handler is part of a secure operating system operable in said secure mode and wherein said non-secure exception handler is part of a non-secure operating system operable in said non-secure mode (claim 2 of the U.S. Patent 7,117,284)

Claim 8 recites Apparatus as claimed in claim 1, wherein said processor is also operable in a monitor mode and any switching between a secure mode and a non-secure mode required for handling of an exception as specified by said parameters takes place via said monitor mode, said processor being operable at least partially in said monitor mode to execute a monitor program to manage switching between said secure mode and said non-secure mode (claims 3 and 4 of the U.S. Patent 7,117,284)

Claim 11 recites A method of processing data, said method comprising the steps of: executing a program with a processor operable in a plurality of modes and a plurality of domains, said plurality of domains comprising a secure domain or a non-secure domain, said plurality of modes including: at least one secure mode being a mode in said secure domain; and at least one non-secure mode being a mode in said non-secure domain; wherein when said processor is executing a program in a secure mode said program has access to secure data which is not accessible when said processor is operating in a non-secure mode; in response to one or more exception conditions triggering exception processing using an exception handler; wherein said processor selects an exception handler in response to one or more parameters specifying which of said exceptions should be handled by a secure mode exception handler executing in a secure mode and which of said exceptions should be handled by an exception handler executing in a mode within a current one of said secure domain and said non-secure domain when that exception occurs (claim 6 of the U.S. Patent 7,117,284)

Claim 15 recites a method as claimed in claim 11, wherein at least one of said parameters is a signal value provided at a hardware input to said processor (claim 10 of the U.S. Patent 7,117,284).

Claims 16 and 17 recite a method as claimed in claim 11, wherein said secure exception handler is part of a secure operating system operable in said secure mode and wherein said non-secure exception handler is part of a non-secure operating system operable in said non-secure mode (claim 7 of the U.S. Patent 7,117,284)

Claim 18 recites A method as claimed in claim 11, wherein said processor is also operable in a monitor mode and any switching between a secure mode and a non-secure mode required for handling of an exception as specified by said parameters takes place via said monitor mode, said processor being operable at least partially in said monitor mode to execute a monitor program to manage switching between said secure mode and said non-secure mode (claims 8 and 9 of the U.S. Patent 7,117,284).

Claim 21 recites a computer program product having a computer program operable to control a data processing apparatus in accordance with the method of claim 11 (claim 11 of the U.S. Patent 7,117,284)

17. Examiner also requests the Applicant to check co-pending applications 10/714,519 (U.S. Pub. No. 2004/0158736) and 10/714,563 (U.S. Pub. No. 2004/0158727) for provisional obviousness-type double patenting rejections.

Response to Arguments

18. Applicant's arguments filed 26 April 2007 have been respectfully and fully considered but they are not persuasive.

19. The amendment to claims 1 and 11 necessitate additional 112 (1^{st}) rejections for claims 1, 3-11 and 13-21.

20. The objection to the specification is maintained because of the reason above under "specification"

21. The 101 rejection is maintained because of the reason above under Claim Rejections - 35 USC § 101

22. The Double patenting rejection is maintained because the Applicant does not respond to the rejection in the first office action. The examiner assumes the Applicant agrees with the examiner on the rejection, therefore, a timely filed terminal disclaimer is needed in order to overcome the rejection.

23. Applicant's arguments are summarized as:

- Regarding the Applicant's argument on page 9 of the remark, "Claim 1 has been amended based on the features of now-canceled claim 2, and claim 11 has been amended based on the features of now-canceled claim 12" and "The claimed exception trap mask register allows the nature...to be **programmed**", the examiner respectfully disagrees.

First, The examiner respectfully points out the amended claims 1 and 11 recite "...stored in a **programmable** exception trap mask register...". However, the canceled claims 2 and 12, recite "...stored in an exception trap mask register". Please note "**programmable** exception trap mask register" and "exception trap mask" are not the same.

Second, for the sake of argument, even if "programmable exception trap mask register" is disclosed in the original disclosure, the Applicant is respectfully reminded that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns, 988 F. 2d 1181, 26 USPQ 2d 1057 (Fed. Cir. 1993).*

Third, Christie et al. does teach "said processor being responsive to one or more parameters stored in a programmable exception trap mask register, said one or more parameters..." by disclosing "...**Redirection** of interrupts in exception logic 170 may be enabled and disabled depending on the state of a **SEM enable signal 401**...In one embodiment, SEM enable signal 401 may be derived from **an SEM enable flag** (not shown) in **a designated control register or a model specific register** that may be asserted during a secure initialization process" – e.g. col. 10, line 12 – col. 11, line 8 and "...In one embodiment, SEM features may be **disabled** by deasserting **an SEM enable flag** (not shown) in a

designated control register or a model specific register (block 514). Once SEM features are disabled, the SK may cause the INIT interrupt to be reissued and normal processing of INIT proceeds as described above (block 515)" – e.g. col. 11, lines 57- col. 12, line 4.

- Regarding Applicant's argument that "Christie's register does not store any parameter specifying whether or not that interrupt is to be redirected..." on pages 9-10 of the remark, the examiner respectfully disagrees.

  Christie et al. discloses store any parameter specifying whether or not that interrupt is to be redirected by disclosing "...**Redirection** of interrupts in exception logic 170 may be enabled and disabled depending on the state of a **SEM enable signal 401**...In one embodiment, SEM enable signal 401 may be derived from **an SEM enable flag** (not shown) in **a designated control register or a model specific register** that may be asserted during a secure initialization process" – e.g. col. 10, line 12 – col. 11, line 8 and "...In one embodiment, SEM features may be **disabled** by deasserting **an SEM enable flag** (not shown) in a **designated control register or a model specific register** (block 514). Once SEM features are disabled, the SK may cause the INIT interrupt to be reissued and normal processing of INIT proceeds as described above (block 515)" – e.g. col. 11, lines 57- col. 12, line 4.

Conclusion

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to April Y. Shan whose telephone number is (571) 270-1014. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Y. Vu can be reached on (571) 272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

9 July 2007
AYS

KIM VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100